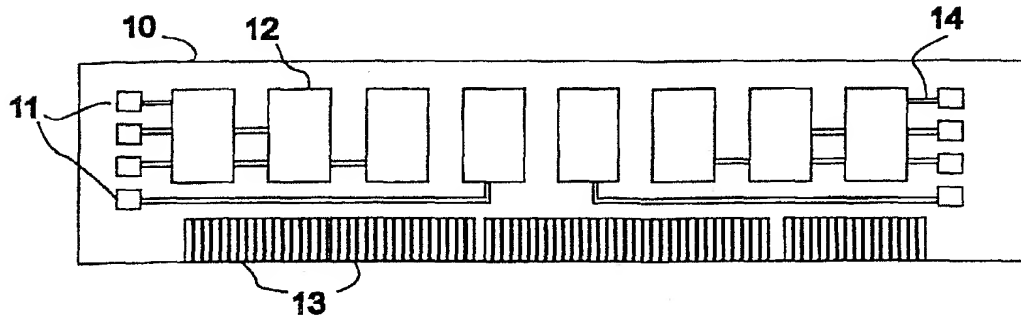
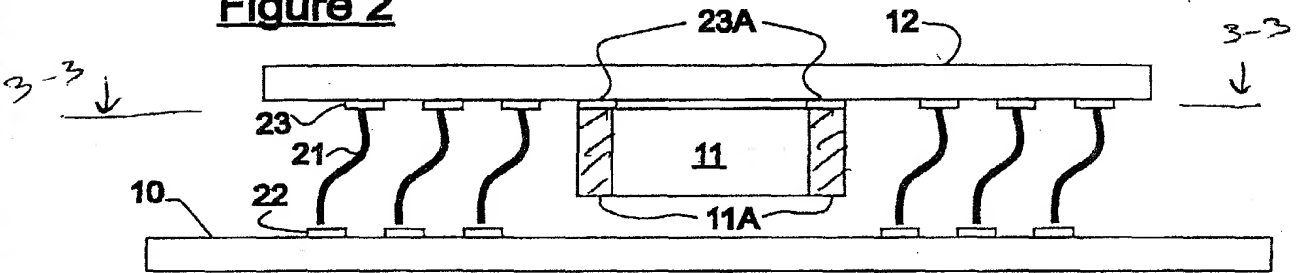


**Figure 1**

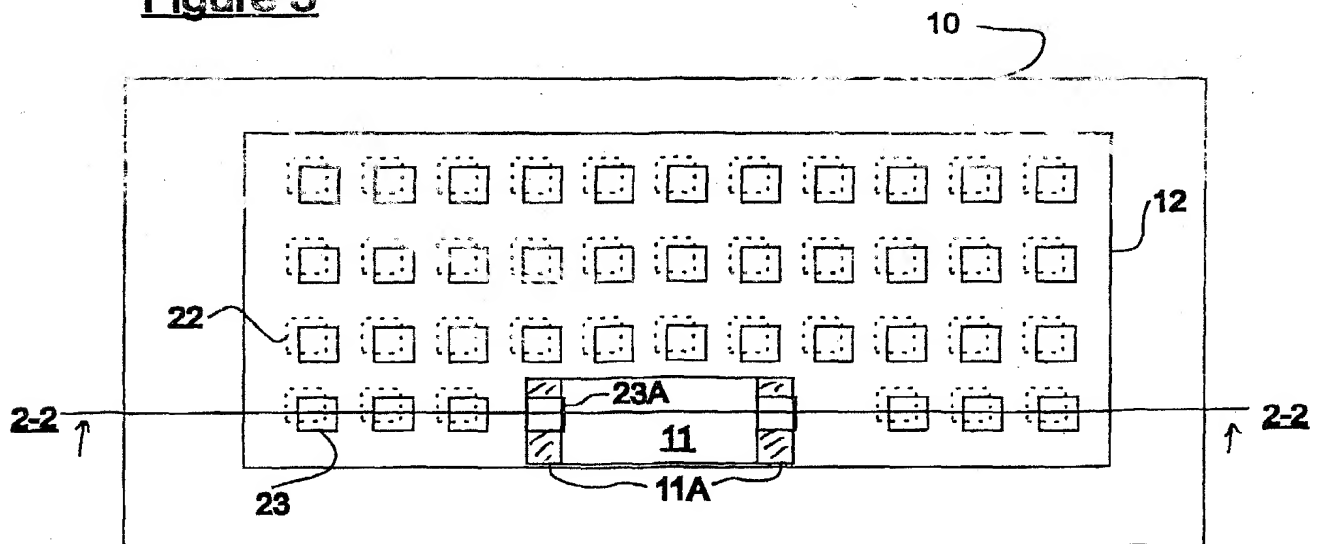
**PRIOR ART**



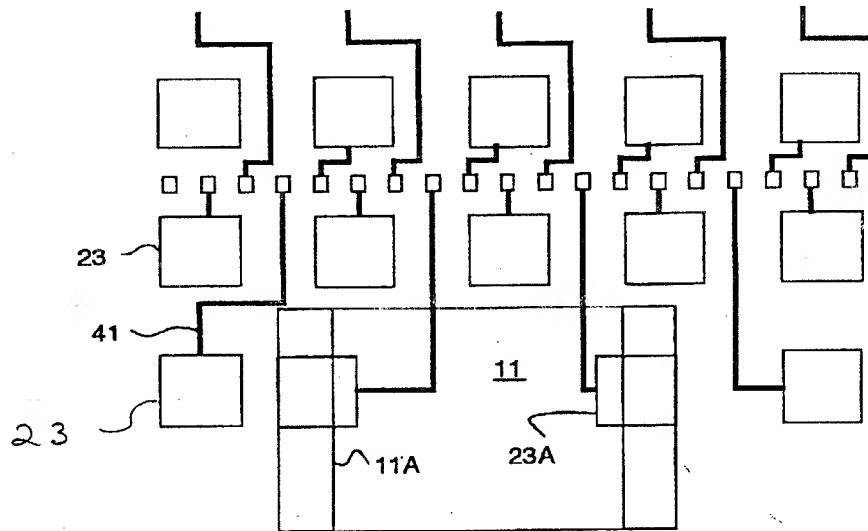
**Figure 2**



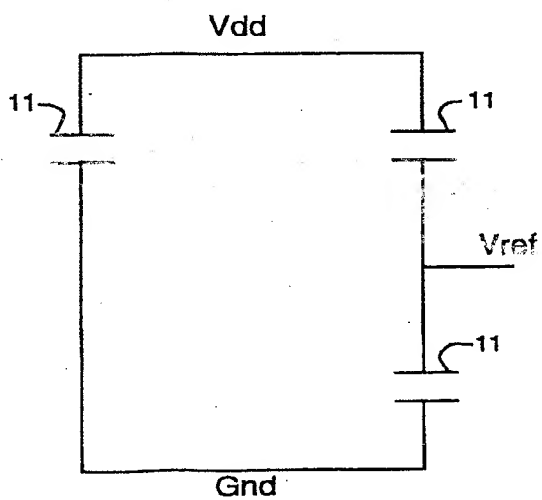
**Figure 3**



**Figure 4A**



**Figure 7A**



**Figure 7B**

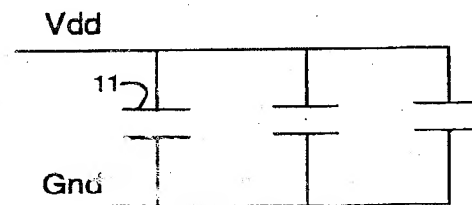


Figure 4B

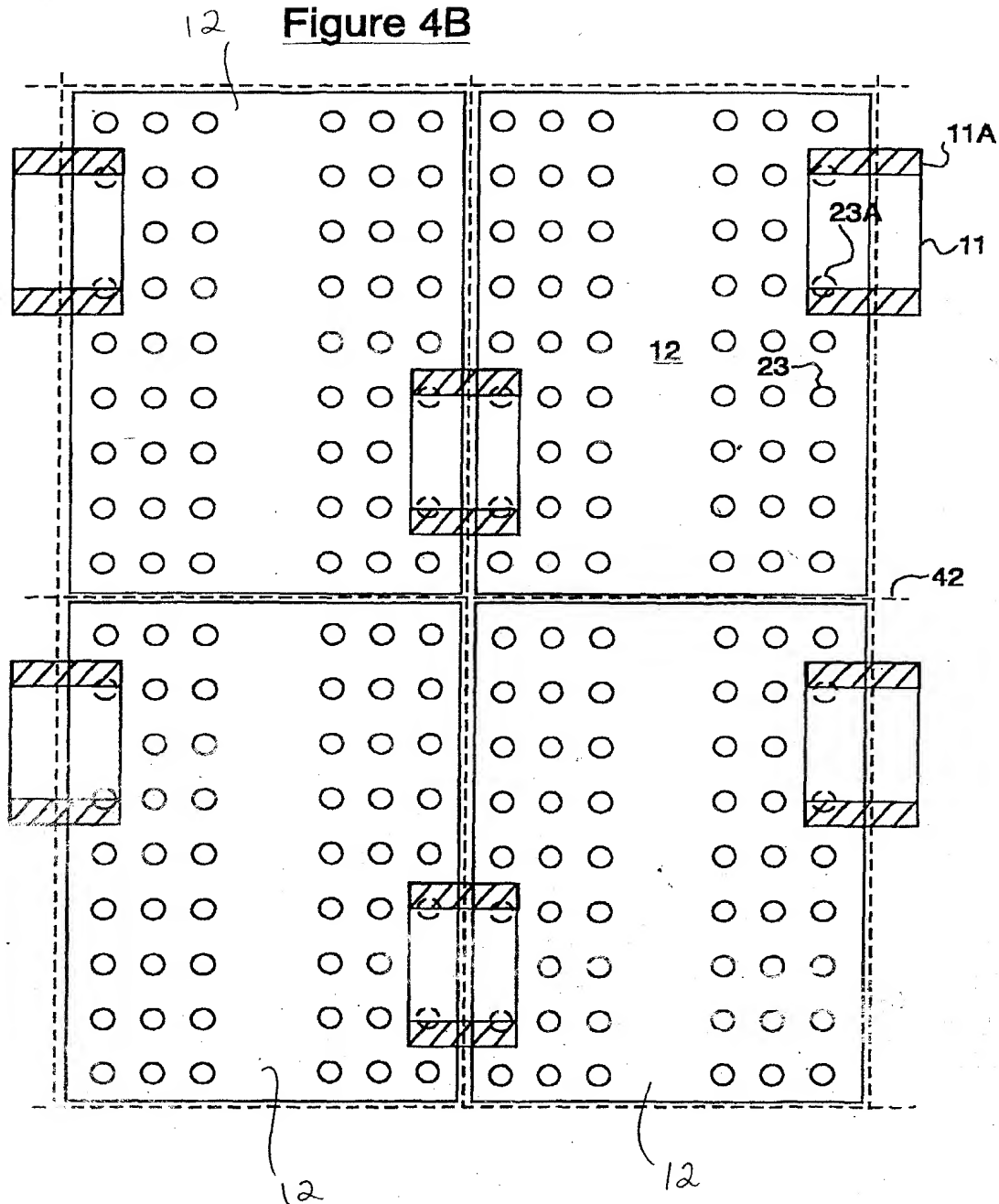




FIG. 8A

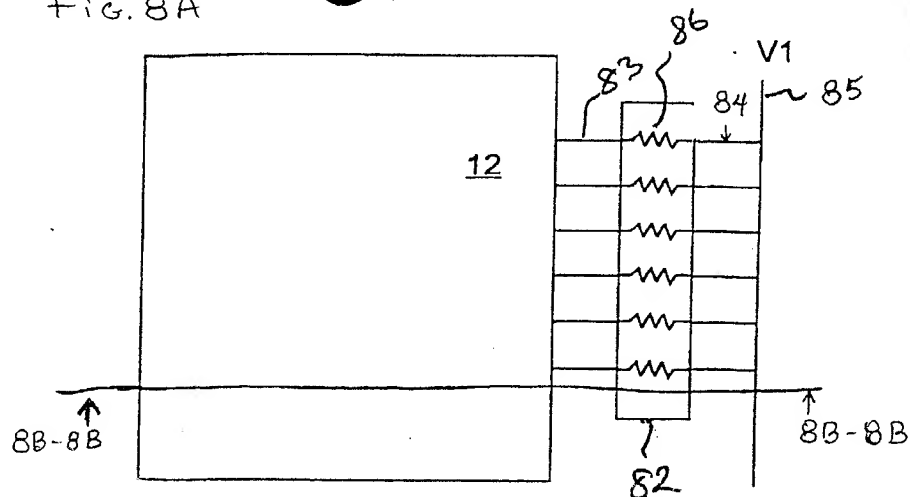
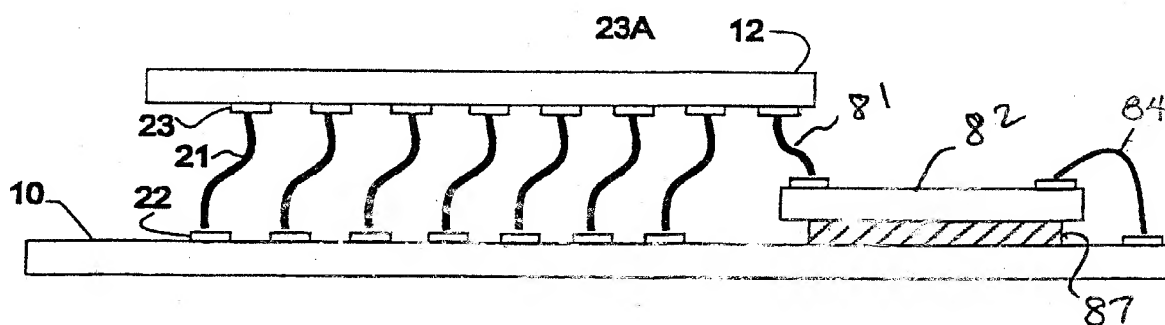


Figure 8B





**Figure 11**  
(Prior Art)

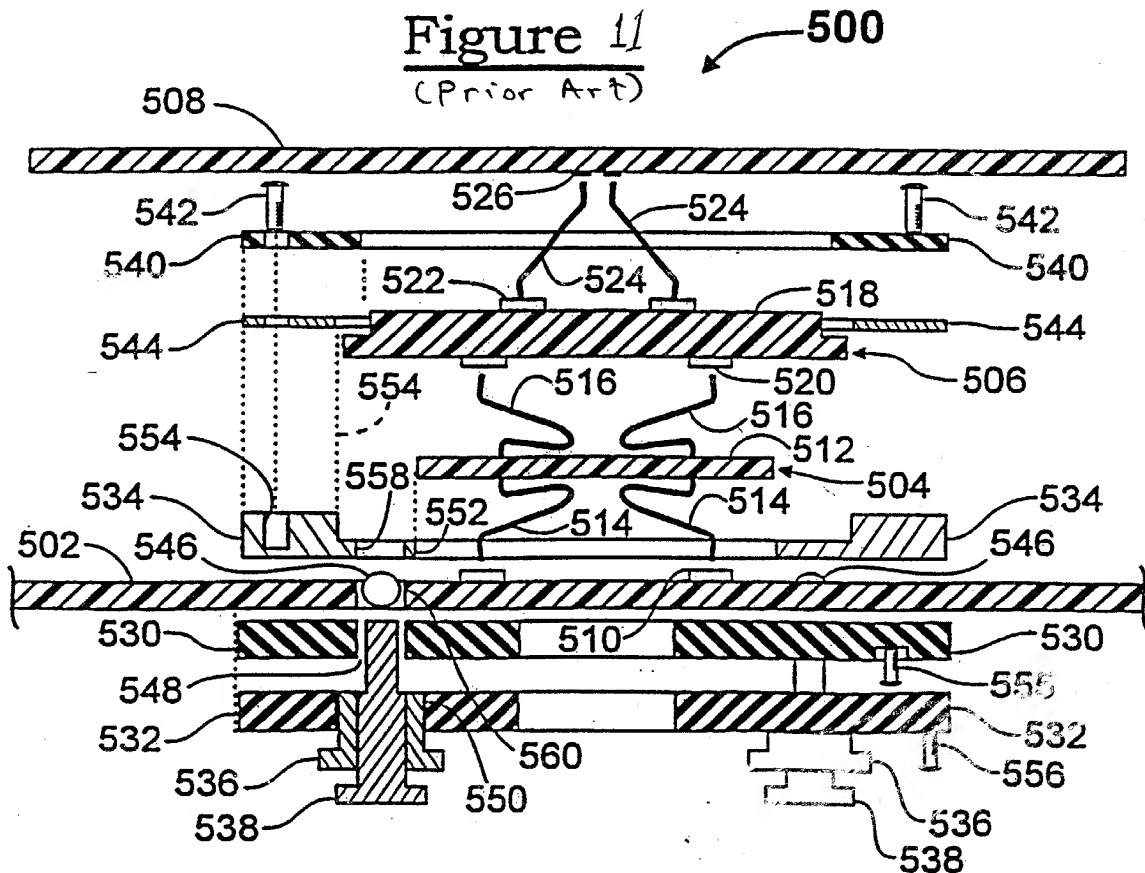


Figure 12 A  
(Prior Art)

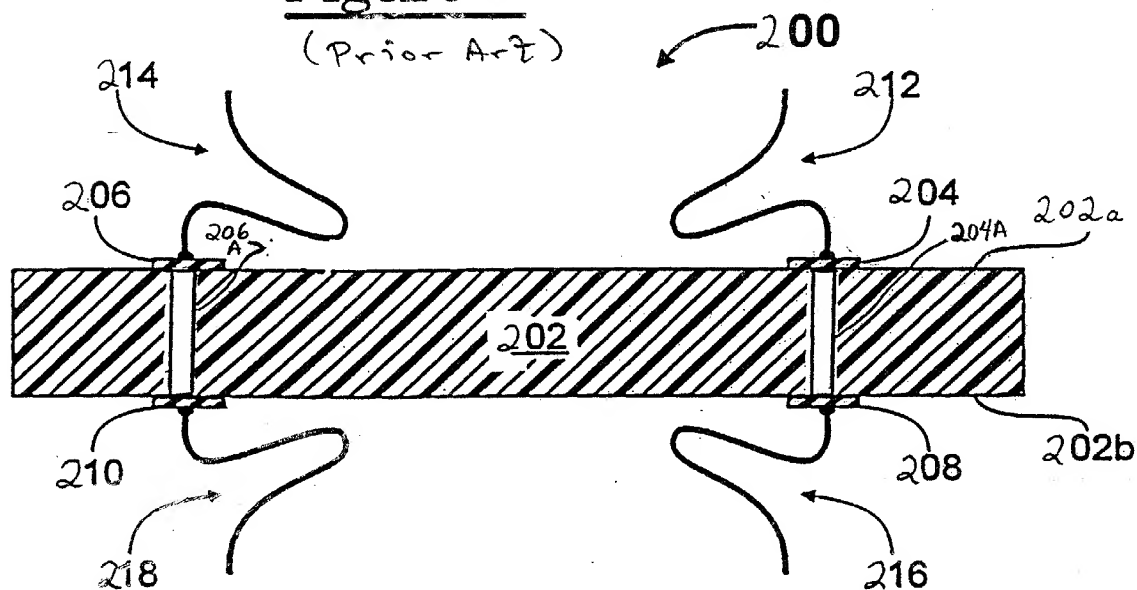


FIG. 12A



FIG. 12B (Prior Art)

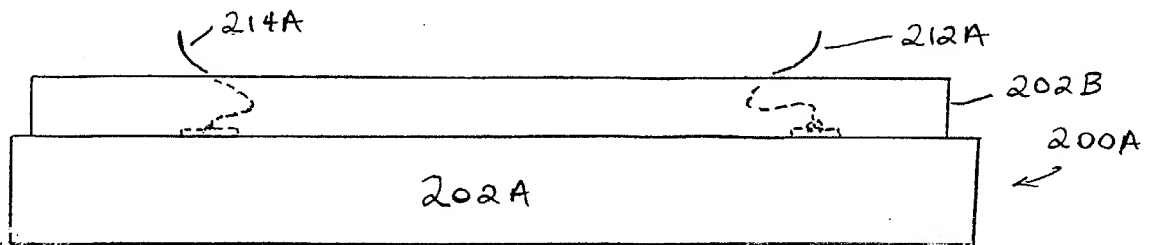


FIG. 12C (Prior Art)

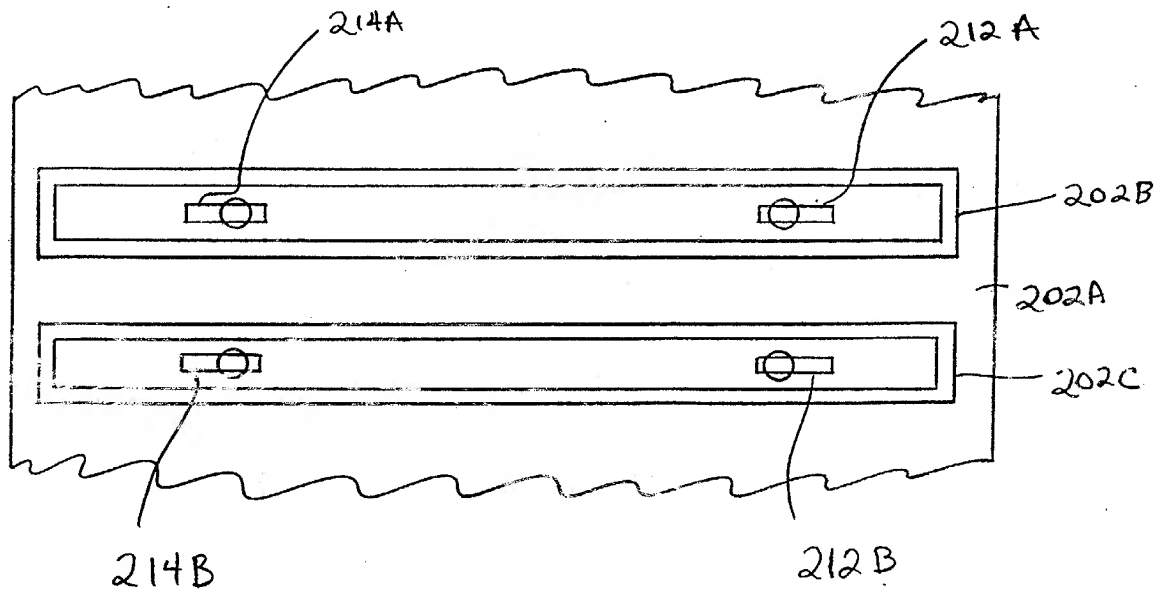


Figure 13 A (Prior Art)

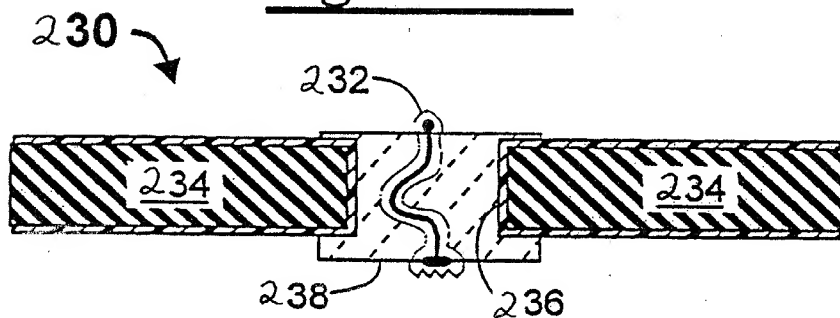
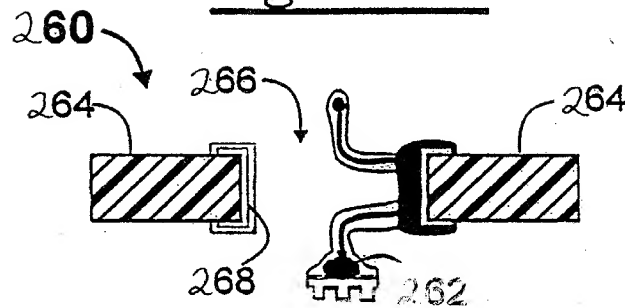


Figure 13 B (Prior Art)



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FIG. 14 (Prior Art)

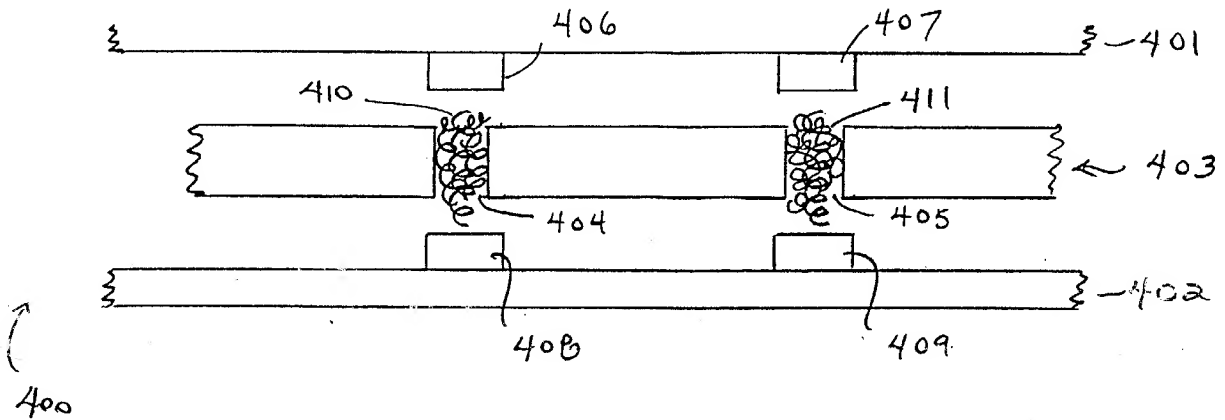


FIG. 14 (Prior Art)

Figure 15A

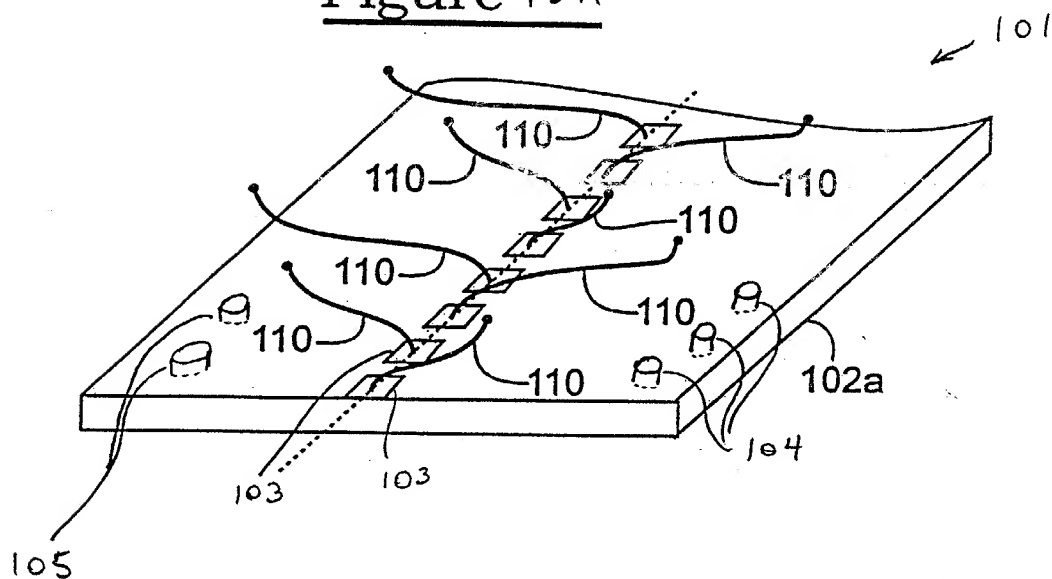


FIG. 15B

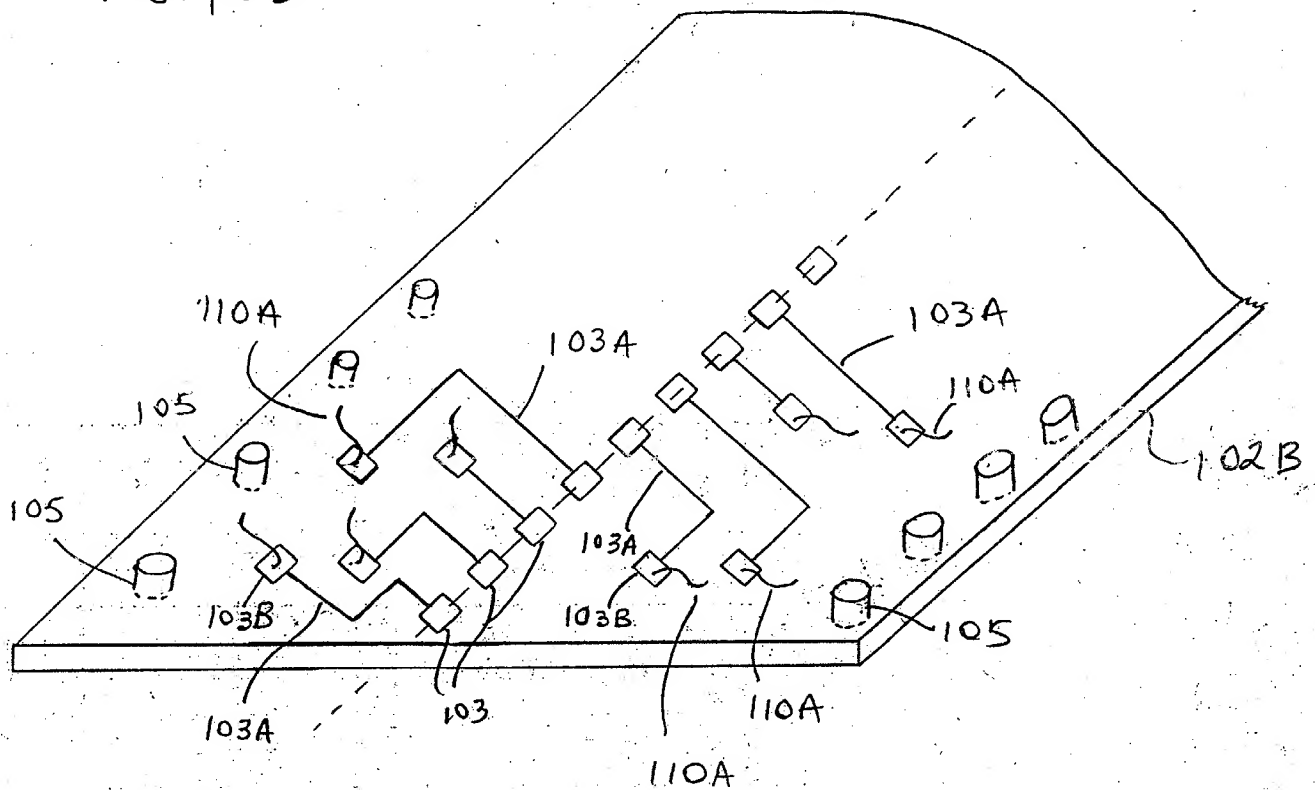


FIG. 15B

FIG. 16 A

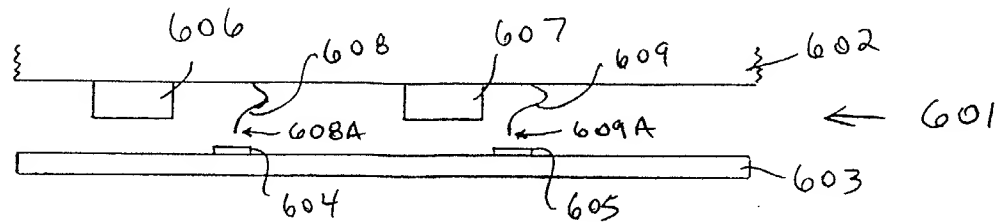


FIG. 16 B

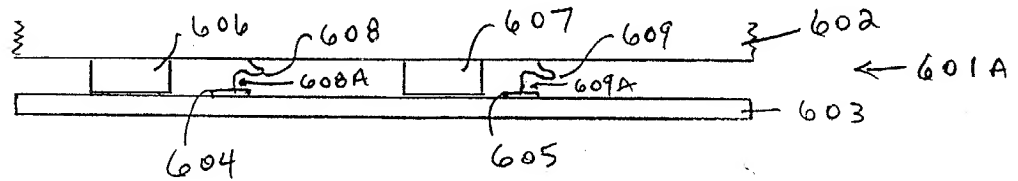


FIG. 17

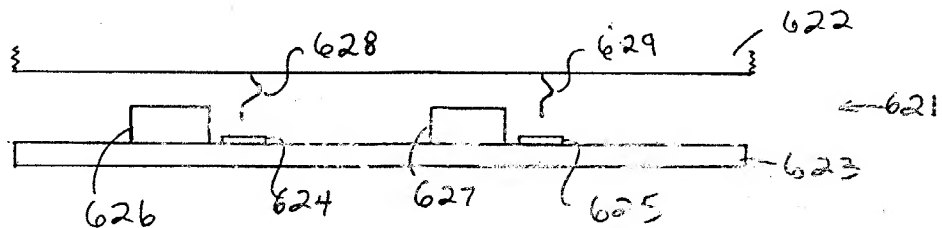


FIG. 16C

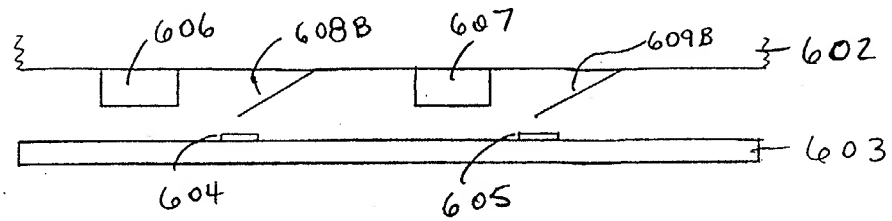


FIG. 16D

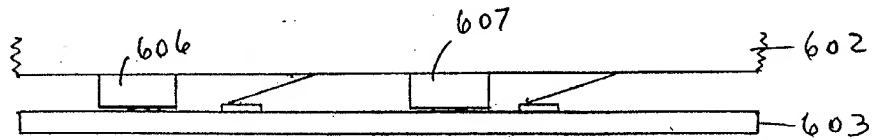


FIG. 16C



FIG. 18 A

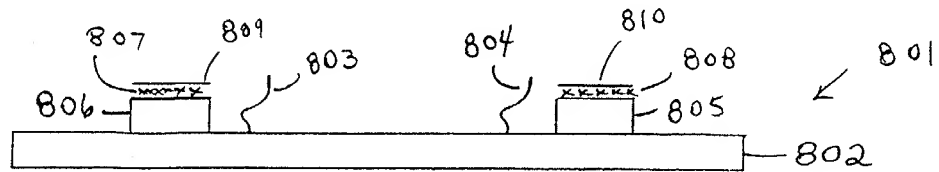
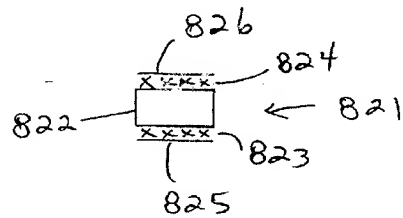


FIG. 18 B



TOP SECRET

A cross-sectional view of a semiconductor device 1401. The device is built on a substrate 1403. A gate stack 1402 is formed on the substrate, with a gate electrode 1404 and a gate insulating layer 1403A. The gate stack is divided into two regions by a trench 1405. The left region contains a transistor 1421 with a gate electrode 1427 and a source/drain region 1429. The right region contains a transistor 1411 with a gate electrode 1415 and a source/drain region 1413. The source/drain regions are connected to a common source/drain region 1423. The device is biased with  $V_{ss}$  and  $V_{dd}$ .